AMENDMENTS

Amendments to the Claims are reflected in the Listing of the Claims that begins on page 2 of this paper. Remarks begin on page 11 of this paper.

In the Claims:

Please cancel claims 1-16 without prejudice.

Listing of the Claims:

Claims 1-16 (canceled).

Claims 17-25 (withdrawn).

Claim 26 (new): A method of constructing an electrical contact on a first electrical component, comprising the steps of:

on an electronic chip including an interconnection surface, the interconnection surface including a plurality of exposed contact pads and a non-wetting surface between the contact pads, fabricating on each of a portion of or all of the contact pads a protruding electrically conducting core having a solder wettable surface; and

bringing the entire interconnection surface in contact with molten solder, thereby depositing solder on all of the cores to form solder bumps thereon and leaving a substantial absence of solder between the cores.

Claim 27 (new): A method according to claim 26, wherein the electrically conducting core includes a metal stud.

Claim 28 (new): A method according to claim 27, wherein said fabricating a protruding electrically conducting core is performed by bonding a wire to a contact pad.

Claim 29 (new): A method according to claim 28, wherein the protruding electrically conducting core is formed by a gold wire of about 25.4 μm diameter.

Claim 30 (new): A method according to claim 27, further comprising the step of coining the metal studs after fabrication on the contact pads.

Claim 31 (new): A method according to claim 27, further comprising the step of stacking a plurality of studs by wire bonding.

Claim 32 (new): A method according to claim 26, wherein the formed solder bumps have a dimension of 75 μm or less without any bridging in-between.

Claim 33 (new): A method according to claim 26, wherein the step of bringing the entire interconnection surface in contact with molten solder is performed by dipping the interconnection surface into a bath of molten solder.

Claim 34 (new): A method according to claim 26, wherein the step of bringing the entire interconnection surface in contact with molten solder is performed through a wave soldering process.

Claim 35 (new): A method according to claim 26, wherein the contact pads are spaced at a pitch of about 150 μm or less.

Claim 36 (new): A method according to claim 26, wherein the step of bringing the entire interconnection surface in contact with molten solder is performed on a plurality of electronic chips on the same wafer.

Claim 37 (new): A method according to claim 36, further comprising the step of:

following the step of bringing the entire interconnection surface in contact with molten solder, dicing the wafer into individual chips.

Claim 38 (new): A method according to claim 26, further comprising the step of repeating the contact of the interconnection surface with molten solder to increase the size of the solder bumps.

Claim 39 (new): A method of electrically connecting the produced chip of claim 26 to a second electronic component, the second electronic component having corresponding solderable contacts positioned to mate with the contacts of the first electrical component, the method further comprising the steps of:

mating the first and second electronic components such that the corresponding contacts of both the first and second electronic components are brought into proximal alignment; and

applying heat to make an electrical connection between the corresponding contacts of the first and second electronic components using the solder of the solder bumps of the first electronic component.

Claim 40 (new): A method according to claim 26, wherein the electrically conducting core is formed from a material selected from the group consisting of gold, copper, silver, platinum, palladium and nickel and their alloys.

Claim 41 (new): A method according to claim 26, wherein the electrically conducting core is coated with a material selected from the group consisting of gold, copper, silver, platinum, palladium and nickel and their alloys.

Claim 42 (new): A method of constructing electrical contacts on a wafer whereon is fabricated a number of semiconductor chips, each chip having an interconnection surface on the same side of the wafer, each interconnection surface including a plurality of exposed contact pads and a non-wetting surface between the contact pads, the method comprising the steps of:

fabricating on each of a portion of or all of the contact pads a protruding metal stud having a solder wettable surface;

simultaneously bringing the entire interconnection surface of chips of the wafer in contact with molten solder, thereby depositing solder on all of the studs to form solder bumps thereon and leaving a substantial absence of solder between the studs; and

following the step of bringing the entire interconnection surface of the wafer in contact with molten solder, dicing the wafer into separate and individual chips.

Claim 43 (new): A method according to claim 42, wherein said fabricating a protruding stud is performed by bonding a wire to the particular contact pad.

Claim 44 (new): A method according to claim 43, wherein the protruding stud is formed by a gold wire of about 25.4 μm diameter.

Claim 45 (new): A method according to claim 42, further comprising the step of coining the metal studs after fabrication on the contact pads.

Claim 46 (new): A method according to claim 42, further comprising the step of stacking a plurality of studs by wire bonding.

Claim 47 (new): A method according to claim 42, wherein the formed solder bumps have a dimension of 75μm or less without any bridging in-between.

Claim 48 (new): A method according to claim 42, wherein the step of bringing the entire interconnection surface in contact with molten solder is performed by dipping the interconnection surface into a bath of molten solder.

Claim 49 (new): A method according to claim 42, wherein the step of bringing the entire interconnection surface in contact with molten solder is performed through a wave soldering process.

Claim 50 (new): A method according to claim 42, wherein the contact pads are spaced at a pitch of about 150μm or less.

Claim 51 (new): A method according to claim 42, further comprising the step of repeating the contact of the interconnection surface with molten solder to increase the size of the solder bumps.

Claim 52 (new): A method of electrically connecting the produced separated chip of claim 42 to a second electronic component, the second electronic component having corresponding solderable contacts positioned to mate with the contacts of the separated chip, the method further comprising the steps of:

mating the separated chip and second electronic component such that the corresponding contacts of both are brought into proximal alignment; and

applying heat to make an electrical connection between the contacts of the separated chip and second electronic component using the solder of the solder bumps of the separated chip.

Claim 53 (new): A method according to claim 42, wherein the electrically conducting core is formed from a material selected from the group consisting of gold, copper, silver, platinum, palladium and nickel and their alloys.

Claim 54 (new): A method according to claim 42, wherein the electrically conducting core is coated with a material selected from the group consisting of gold, copper, silver, platinum, palladium and nickel and their alloys.

Claim 55 (new): A method of constructing electrical contacts on a wafer whereon is fabricated a number of semiconductor chips, each chip having an interconnection surface on the same side of the wafer, each interconnection surface including a plurality of exposed contact pads and a non-wetting surface between the contact pads, the contact pads being spaced at a pitch of about 150 μm or less, the method comprising the steps of:

fabricating on each of a portion of or all of the contact pads a protruding metal stud having a solder wettable surface by bonding a wire to the contact pads;

coining the metal studs;

simultaneously bringing the entire interconnection surface of chips of the wafer in contact with molten solder through a solder bath or wave solder process, thereby depositing solder on all

of the studs to form solder bumps having a dimension of 75 μm or less without any bridging in-between; and

following the step of bringing the entire interconnection surface of the wafer in contact with molten solder, dicing the wafer into separate and individual chips.

Claim 56 (new): A method according to claim 55, wherein the protruding stud is formed by a gold wire of about 25.4 μm diameter.

Claim 57 (new): A method according to claim 55, further comprising the step of stacking a plurality of studs by wire bonding.

Claim 58 (new): A method according to claim 55, further comprising the step of repeating the contact of the interconnection surface with molten solder to increase the size of the solder bumps.

Claim 59 (new): A method according to claim 55, wherein the electrically conducting core is formed from a material selected from the group consisting of gold, copper, silver, platinum, palladium and nickel and their alloys.

Claim 60 (new): A method according to claim 55, wherein the electrically conducting core is coated with a material selected from the group consisting of gold, copper, silver, platinum, palladium and nickel and their alloys.